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APPLICANTS Katsuhiro Nakai, Sanda-shi, JAPAN; Tsuyoshi Nanba, Hirakata-shi, JAPAN; Takehisa Hirano, Mino-shi, JAPAN; Tomoaki Tezuka, Osaka-shi, JAPAN;				
** CONTINUING DATA ***** This application is a 371 of PCT/JP03/07541 06/13/2003				
** FOREIGN APPLICATIONS ***** JAPAN 2002-174883 06/14/2002				
Foreign Priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 (a-d) conditions <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance		STATE OR COUNTRY JAPAN	SHEETS DRAWING 12	TOTAL CLAIMS 44
Verified and Acknowledged <u> </u> Examiner's Signature <u> </u> Initials		INDEPENDENT CLAIMS 16		
ADDRESS 513				
TITLE Semiconductor intergrated circuit device, data storage verification device, and data storage verification method				
FILING FEE RECEIVED 2526	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit	